an oxide layer formed on a side wall of the first gate electrode; and

a first nitride spacer formed on the oxide layer;

a second nitride spacer formed on the side wall of the device isolation film;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode; and

second and third insulating films filling and planarizing the space above the active region and between the gate electrode structure and the second nitride spacer.

See the attached Appendix for the changes made to effect the above claim(s).